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328812(28)

APR-MAY

B. E. (Eight Semester) Examination, 2020

(Old Scheme)

(Et & T Engg. Branch)

VLSI DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Part (a) of each question is compulsory. Attempt any* ***two*** *parts from (b), (c) and (d).*

Unit-I

1. (a) Define CPLD. 2

(b) What are differences in SSI, MSI and LSI? 7

(c) Explain VLSI Design flow chart with diagram. 7

(d) Explain FPGA architecture with block diagram. 7

Unit-II

2. (a) Define Bi-CMOS 2

(b) Explain PMOS fabrication process 7

(c) What are the main point of Lambda based design rule? Explain it. 7

(d) Draw schematic and stick diagram for 2 input CMOS NOR Gate. 7

Unit-III

3. (a) Define Layout. 2

(b) Draw and explain 4 × 4 NAND-ROM layouts. 7

(c) Draw and explain layout of JK flip flop. 7

(d) Construct layout for 1 bit full adder. 7

Unit-IV

4. (a) Define VHDL. 2

(b) Explain the static and dynamic power dissipation in CMOS inverter. 7

(c) Explain different type Architecture body in VHDL. 7

(d) What is entity in VHDL? Explain the entity declaration. 7

Unit-V

5. (a) Define "process" in VHDL. 2

(b) Write VHDL code for D-flip flops. 7

(c) Explain inertial delay model and transport delay model in VHDL. 7

(d) Write the comparison of Moore and Mealy FSM. 7